ABSTRACT OF THE DISCLOSURE

A video signal processor and a video signal processing method which can prevent the length of one period of a clock from being shortened and can output a video signal that is in phase with a reference signal. When a video data signal that has been processed using a first clock signal is processed using a second clock signal, this video signal processor does not utilize as the second clock signal, a clock signal that is in phase with a reference signal but a clock signal that is employed in a later stage signal processor, and interpolates the video data signal by an interpolation circuit so as to make the signal in phase with the reference signal.